AMENDMENTS TO THE CLAIMS

1. (Original) An interpolation filter for processing a sequence of input samples provided at an input rate controlled by an input clock, so as to generate interpolants at an output rate controlled by an output clock, which is substantially independent of the input clock, the filter comprising a plurality of stages arranged in a succession in which each of the stages, except for a first stage in the succession, is coupled respectively to a preceding one of the stages, each of the stages comprising:

a multiplier, coupled to receive the input samples and to multiply each of the samples by a respective coefficient determined responsive to a phase interval between the input clock and the output clock, so as to generate an interpolation product; and

a multiplexer-accumulator, coupled to add the interpolation product, in synchronization with the input clock, to an interim value stored by the multiplexer-accumulator and, except for the first stage, further coupled to receive, in synchronization with the output clock, the interim value stored by the preceding stage, thereby generating the interpolants at an output of the multiplexer-accumulator of a last stage in the succession.

2. (Original) A filter according to claim 1, wherein the stages are arranged so as to constitute a finite impulse response (FIR) filter, and wherein the coefficient is determined based on a predetermined response of the filter.

3. (Original) A filter according to claim 1, and comprising a memory, adapted to store values of the coefficient at addresses in the memory corresponding to respective values of the phase interval, and coupled to output the values to the multiplier responsive to the address.

4. (Original) A filter according to claim 3, and comprising a coefficient interpolator, coupled to receive at least two of the values from the memory corresponding to approximate values of the phase interval and to calculate an exact value of the coefficient by interpolation between the approximate values.

5. (Original) A filter according to claim 1, wherein for any given value of the phase interval, the coefficient is substantially invariant with respect to the input rate.

6. (Original) A filter according to claim 1, wherein for any given value of the phase interval, the coefficient is substantially invariant with respect to the output rate.

7. (Original) A filter according to claim 1, wherein the multiplexer-accumulator comprises:

a register, adapted to store the interim value;

an adder, coupled to receive and sum the interpolation product and the interim value; and

a multiplexer, having a first input coupled to the adder and, except for the first stage, a second input coupled to the preceding stage and an output coupled to the register, wherein the multiplexer is operative to select the first input responsive to the input clock and the second input responsive to the output clock.

8. (Original) A filter according to claim 7, wherein the second input of the first stage is coupled so as to zero the interim value stored in the register of the first stage responsive to the output clock.

9. (Original) A filter according to claim 1, wherein the input samples are generated by sampling, at the input rate, an input signal of a receiver, the input signal carrying a stream of symbols generated by a transmitter at a symbol rate, wherein the output rate is synchronized with the symbol rate.

10. (Original) A filter according to claim 9, wherein the output rate is synchronized with the symbol rate irrespective of the input rate.

11. (Currently amended) A multichannel communication device, comprising:

an input unit, coupled to a plurality of communication lines for carrying signals at respective baud rates, and operative to transfer the signals received on the lines at an input rate determined by a common system clock, substantially unsynchronized with the baud rates of at least some of the lines; and

a plurality of digital processing channels, each coupled to the input unit so as to receive the signals at the input rate from a respective one of the lines and to process the signals so as to output symbols at one of the baud rates that is applicable to the signals carried on the respective one of the lines.

12. (Original) A device according to claim 11, wherein the input unit comprises an analog front end, which is operative to sample the signals at the input rate and to convey the sampled signals to the digital processing channels.

13. (Original) A device according to claim 12, wherein the device comprises a modem, and wherein the signals comprise input signals, which are received from the communication lines, and output signals, which are transmitted over the communication lines by the digital processing channels via the analog front end.

14. (Original) A device according to claim 11, wherein the plurality of digital processing channels comprises at least first and second channels, which are adapted to process the signals so as to output symbols at different, respective first and second baud rates.

15. (Original) A device according to claim 14, wherein the first and second channels are configured to output the symbols in synchrony with respective first and second symbol clocks, which are mutually substantially unsynchronized.

16. (Original) A device according to claim 11, wherein each of the digital processing channels comprises a digital interpolation filter, which is coupled to process a sequence of input samples of the received signals provided at the input rate, and to generate interpolants at an output rate determined by an output clock in synchrony with the baud rate, for use in recovering the output symbols.

17. (Original) A device according to claim 16, wherein the filter comprises a plurality of stages arranged in a succession in which each of the stages, except for a first stage in the succession, is coupled respectively to a preceding one of the stages, each of the stages comprising:

a multiplier, coupled to receive the input samples and to multiply each of the samples by a respective coefficient determined responsive to a phase interval between the system clock and the output clock, so as to generate an interpolation product; and

a multiplexer-accumulator, coupled to add the interpolation product, in synchronization with the system clock, to an interim value stored by the multiplexer-accumulator and further coupled, except for the first stage, to receive, in synchronization with the output clock, the interim value stored by the preceding stage, thereby generating the interpolants at an output of the multiplexer-accumulator of a last stage in the succession.

18. (Original) A device according to claim 16, wherein each of the digital processing channels comprises:

a number-controlled oscillator (NCO), adapted to determine a fractional interval indicative of a phase offset between the system clock and the output clock, for use in driving the digital interpolation filter; and

transmission circuitry, comprising a transmission interpolation filter, which is coupled to generate output samples for transmission over the communication lines, driven by the fractional interval determined by the NCO.

19. (Original) A method for filtering a signal so as to generate interpolants at an output rate controlled by an output clock, the method comprising:

receiving a sequence of input samples at an input rate controlled by an input clock, substantially independent of the output clock;

processing the samples in a plurality of stages arranged in a succession, each of the stages, except for a last stage in the succession, being coupled respectively to a succeeding one of the stages, the processing comprising in each of the stages:

multiplying each of the samples by a respective coefficient determined responsive to a phase interval between the input clock and the output clock, so as to generate an interpolation product;

in synchronization with the input clock, adding the interpolation product to an interim value stored at the stage; and

in synchronization with the output clock, transferring the interim value to the succeeding stage, thereby generating the interpolants at the last stage; and

outputting the interpolants from the last stage in the succession.

20. (Original) A method according to claim 19, wherein the stages are arranged so as to constitute a finite impulse response (FIR) filter, and wherein multiplying each of the samples comprises determining the coefficient based on a predetermined response of the filter.

21. (Original) A method according to claim 19, wherein determining the coefficient comprises storing values of the coefficient at addresses in a memory corresponding to respective values of the phase interval, and recalling the values for multiplication thereof responsive to the address.

22. (Original) A method according to claim 21, wherein recalling the values comprises recalling at least two of the values from the memory, corresponding to approximate values of the phase interval, and wherein determining the coefficient comprises computing an exact value of the coefficient by interpolation between the approximate values.

23. (Original) A method according to claim 19, wherein multiplying each of the samples comprises processing the interpolants so as to determine the phase interval for use in determining the respective coefficient.

24. (Original) A method according to claim 19, wherein for any given value of the phase interval, the coefficient is substantially invariant with respect to the input rate.

25. (Original) A method according to claim 19, wherein for any given value of the phase interval, the coefficient is substantially invariant with respect to the output rate.

26. (Original) A method according to claim 19, wherein receiving the sequence of input samples comprises sampling, at the input rate, an input signal of a receiver, the input signal carrying a stream of symbols generated by a transmitter at a symbol rate, and wherein generating the interpolants comprises synchronizing the output rate at which the interpolants are generated with the symbol rate.

27. (Original) A method according to claim 26, wherein synchronizing the output rate comprises synchronizing the output rate with the symbol rate irrespective of the input rate.

28. (Original) A method according to claim 26, wherein receiving the sequence of input samples comprises receiving a plurality of signals having respective symbol rates on a corresponding plurality of communication lines, and wherein synchronizing the output rate comprises synchronizing the output rates of the interpolants with the respective symbol rates of the corresponding communication lines.

29. (Original) A method according to claim 28, wherein processing the samples comprises processing the samples of each of the signals in a respective one of a plurality of processing channels.

30. (Original) A method for multichannel communications, comprising:

receiving signals on a plurality of communication lines having respective baud rates;

transferring the signals received on the lines to a corresponding plurality of digital processing channels at an input rate determined by a common system clock, substantially unsynchronized with the baud rates of at least some of the lines; and

processing the signals in each of the digital processing channels so as to generate output symbols at one of the baud rates that is applicable to the signals carried on the corresponding one of the lines.

31. (Original) A method according to claim 30, wherein receiving the signals comprises receiving analog signals and sampling the analog signals at the input rate, and wherein transferring the signals comprises conveying the sampled signals to the digital processing channels.

32. (Original) A method according to claim 30, wherein the received signals comprise incoming signals, and further comprising transmitting outgoing signals over the communication lines using the digital processing channels.

33. (Original) A method according to claim 30, wherein receiving the signals comprises receiving at least first and second signals at different, respective first and second baud rates, and wherein processing the signals comprises generating the symbols substantially simultaneously in different ones of the digital processing channels at the first and second baud rates.

34. (Original) A method according to claim 33, wherein generating the symbols at the first and second baud rates comprises generating the symbols in synchrony with respective first and second symbol clocks, which are mutually substantially unsynchronized.

35. (Original) A method according to claim 30, wherein processing the signals comprises interpolating among input samples of the signals responsive to a phase interval between the system clock and an output clock synchronized with one of the baud rates.

36. (Original) A method according to claim 35, and further comprising generating output samples for transmission over at least one of the communication lines by interpolating the samples responsive to the phase interval.

37. (Original) An interpolation device for processing a sequence of input samples provided at a given input period, and having an output period that is substantially independent of the input period, the device comprising a finite impulse response (FIR) filter, adapted to process the input samples so as to generate a sequence of intermediate results in the filter at successive times corresponding to the output period, and to update the intermediate results for each of the input samples, and to output as an output sample, once in each output period, the intermediate result that was generated at an earliest one of the successive times among the intermediate results in the filter.

38. (Original) A device according to claim 37, and comprising a timing controller, which is coupled to determine a fractional interval indicative of a phase offset between the input period and the output period, wherein the filter generates and updates the intermediate results responsive to the fractional interval determined by the timing controller.

39. (Original) A method for filtering a sequence of input samples provided at a given input period, comprising:

processing the input samples in a finite impulse response (FIR) filter so as to generate a sequence of intermediate results in the filter at successive times corresponding to an output period of the filter, which is substantially independent of the input period;

updating the intermediate results for each of the input samples; and

outputting as an output sample, once in each output period, the intermediate result that was generated at an earliest one of the successive times among the intermediate results in the filter.

40. (Original) A method according to claim 39, and comprising determining a fractional interval indicative of a phase offset between the input period and the output period, wherein processing and updating the intermediate results comprises computing the intermediate results responsive to the fractional interval.